Implementation of Centroid Defuzzifier Block Using CMOS Circuits

M. Mokarram, A. Khoei, Kh. Hadidi, K. Gheysari

***Abstract*—A voltage input current output multiplier and a current input voltage output divider circuit to realize the centre of gravity defuzzifier strategy is described in this paper. The proposed circuit has a compact architecture operating at higher speed and higher input voltage range compared to previously presented structures. The transistors operate in the both saturation and ohmic regions. The circuit operates with a single supply voltage of 3.3V in a 0.35 μm CMOS technology. The total harmonic distortion (THD) of multiplier is less than 1.1%, the linearity error is also less than 3%, and -3db frequency is more than 180 MHz with voltage input range of $3V_{p-p}$. Simulation results are given to verify the functionality of the proposed circuits.**

***Index Terms*—defuzzifier, multiplier, divider, CMOS**

I. INTRODUCTION

A fuzzy processor consists of four fundamental units, which are the fuzzification unit, decision making logic unit, defunzzification unit, and knowledge base. In the past, most fuzzy processors are implemented by software, but a hard-ware implemented one is more suitable for real-time applications. For hardware realization, the fuzzy processors are almost implemented with digital circuits in the earlier years, but the defuzzification units are usually not included in these designs because the digital multiplier and divider circuits used to realize the centre of gravity (COG) defuzzifier will occupy large chip area. The roles these defuzzifiers should play in these fuzzy processors are usually replaced off-chip microprocessors. Therefore, the bandwidth of a microprocessor dominates the limitation of the speed of a fuzzy processor. For this reason, many circuits have been proposed to realize the fuzzy processors to overcome these shortcomes[2].

The input for the defuzzification process is a fuzzy set and the output is a single number. As much as fuzziness helps the rule evaluation during the intermediate steps, the final output for each variable is generally a single crisp number. So, given a fuzzy set that encompasses a range of output values, we need to return one number, thereby moving from a fuzzy set to a crisp output. Perhaps the most popular defuzzification method is the centroid calculation, which returns the center of area under the curve [3].

In this paper, we propose an analog voltage-mode defuzzifier circuit, which is designed based on the voltage-input current-output four quadrant analog multiplier circuit and current-input voltage-output divider circuit. This circuit takes the advantages of analog approach, like high speed, small chip area; it also has the advantages of fewer adder/subtractor circuits.

II. CIRCUIT DESCRIPTION

There are several defuzzification methods. Below we show the most common ones when rules fire individually. In this paper we optimize the center of area defuzzification method.

A. The Center of Area Method

The center of area generates the center of gravity of the possibility distribution of the inferred fuzzy output. In the case of a discrete universe, the equation is:

$$Z_O = \frac{\sum_{j=1}^{n} \mu_Z(W_j) W_j}{\sum_{j=1}^{n} \mu_Z(W_j)} \quad (1)$$

Where n is the number of quantization levels of the output. The block diagram of this defuzzifier is shown in Fig. 1.

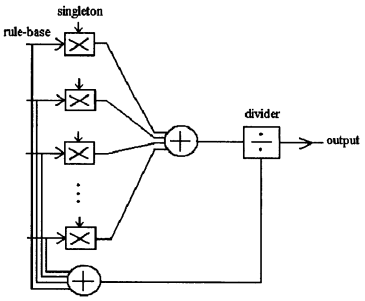

Fig. 1. The block diagram of defuzzifier

As illustrated in Eq. (1) and the block diagram of centroid difuzzifier method, we need divider, multiplier and adder circuits.

B. Quarter-Square Multiplier

The differential squaring circuit is illustrated in Fig.2. One of the input voltages is applied to the gates (x) and the other one to the sources (y) of transistors M1-M4 which are biased with appropriate common-mode voltages X and Y in saturation region. Therefore the drain current of each transistors can be calculated as:

Majid Mokarram najafabad is with Microelectronics Research Laboratory Urmia University, Urmia, Iran (e-mail: st_m.mokarram@urmia.ac.ir).

Abdollah Khoei is with Microelectronics Research Laboratory Urmia University, Urmia, Iran (e-mail: a.khoei@urmia.ac.ir).

Khayrollah Hadidi is with Microelectronics Research Laboratory Urmia University, Urmia, Iran (e-mail: kh.hadidi@urmia.ac.ir).

Kazem Gheysari is with Microelectronics Research Laboratory Urmia University, Urmia, Iran (e-mail: st_k. Gheysari @urmia.ac.ir).

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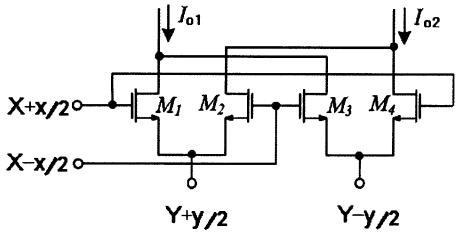

Fig. 2. The multiplier using Differential Squaring Circuit

$$I_d = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)[V_{GS} - V_{TH}]^2 \qquad (2)$$

Where V_{TH} is threshold voltage of NMOS transistors, the differential output current of the circuit proportional to the multiplication of two input signals which is calculated as:

$$I_O = (I_{d1} + I_{d3}) - (I_{d2} + I_{d4}) = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right) \times 2 \times xy \qquad (3)$$

$$I_O = \mu C_{ox}\left(\frac{W}{L}\right)xy \qquad (4)$$

All these transistors have to be biased in saturation region to reach correct answer of above equations. The value of Y+y/2 should be in lower voltage so that the input rang of above multiplier is decreased. To increase the input voltage range and apply biasing of transistors in saturation region we used the circuit that is shown in Fig.3 in the input of above multiplier.

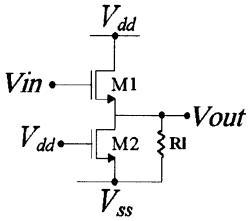

Fig. 3. The input block of multiplier circuit

When the attenuator circuit is used in X input of multiplier, voltage level shifter have to be used at the output of attenuator circuit, so that the attenuator circuit changes to the circuit that is shown in Fig. 4.

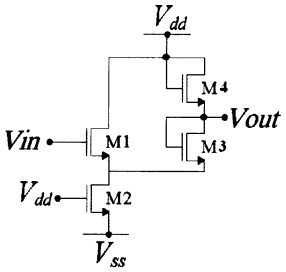

Fig. 4. The input block of multiplier circuit with voltage level shifter

As transistor M1 works in saturation region the output voltage of that circuit becomes:

$$V_{out} = \frac{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L}{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L + \frac{1}{g_m}} \times V_{in} \qquad (5)$$

So the gain of attenuator circuit can be calculated as:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L}{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L + \frac{1}{g_m}} \qquad (6)$$

In above equations $R_L \cong \frac{1}{g_m}$ and $A_V < 1$. So that both input-signals are attenuated before applying to multiplier inputs. A complete wide-range, high-speed voltage-input and current-output analog multiplier can be constructed by above principle as shown in Fig.5.

The proposed multiplier has been simulated using Hspice and level 49 BSIM3V3 parameters. The circuit operates with a single supply voltage of 3.3V in a 0.35 μm CMOS technology. The DC-characteristic of multiplier is shown in Fig. 6. for Vx in x-axis and some different values of Vy from -1.5V to +1.5V

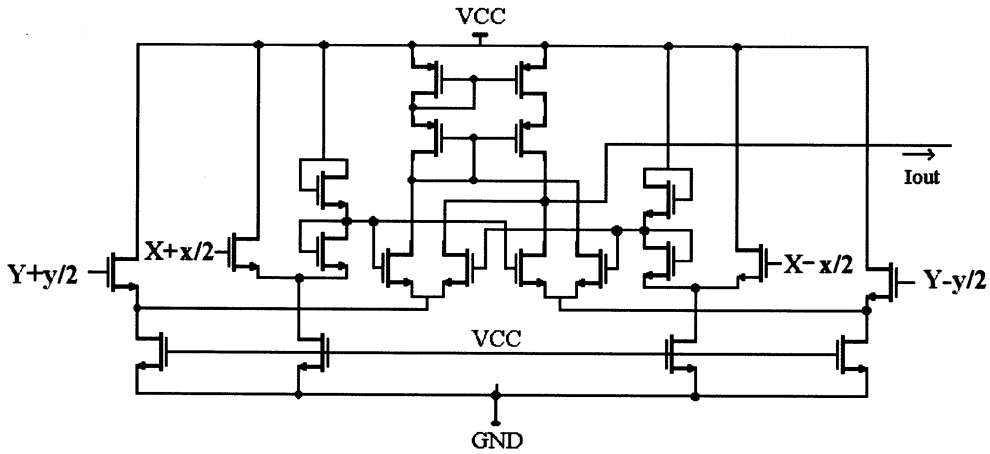

Fig. 5. The complete of wide-range analog multiplier circuit

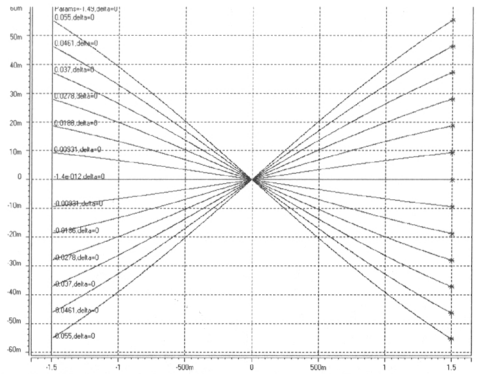

Fig. 6. DC-characteristic of proposed circuit for Vx in x-axis

For constant value of x, the frequency response of proposed circuit is shown in Fig. 7. The band wide is more than 180 Mhz.

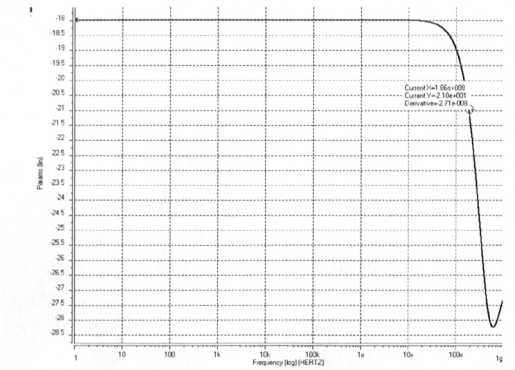

Fig. 7. Bandwidth of proposed multiplier for constant value of x

C. Divider Circuit

The divider circuit is a current-input, voltage-output divider that is shown in Fig. 8 [1]

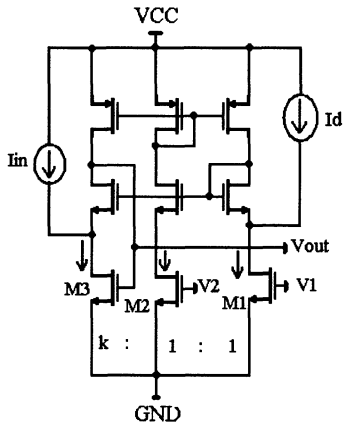

Fig. 8. The Referenced divider circuit

The division is performed by means of transistors M1, M2, M3 at the bottom layer, all of them being constrained to operate in the triode region. While V1 and V2 are fixed bias voltages, the following relations hold for the drain currents of the triode transistors [1]:

$$I_1 = \beta V_{ds}\left(V_1 - V_{TN} - \frac{n}{2}V_{ds}\right) = I_d + I_2 \qquad (7)$$

$$I_2 = \beta V_{ds}\left(V_2 - V_{TN} - \frac{n}{2}V_{ds}\right) \qquad (8)$$

$$I_3 = k\beta V_{ds}\left(V_{out} - V_{TN} - \frac{n}{2}V_{ds}\right) = I_{in} + kI_2 \qquad (9)$$

Where V_{ds} is the common drain-to-source voltage drop for the three bottom transistors while β is the current gain ratio of M1 and M2. Therefore from the three equations (7-9) output equation of divider can be written as:

$$(V_{out} - V_2) = \frac{(V_1 - V_2)}{k}\frac{I_{in}}{I_d} \qquad (10)$$

The circuit in Fig. 8 has been simulated as Fig. 9 which shows the variation of the output voltage V_{out} as a function of the numerator current I_{IN} for different values of the denominator currents I_D.

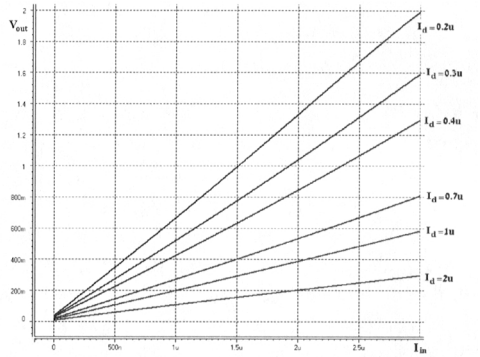

Fig .9. Simulation results for the divider circuit.

D. Transconductor Circuit

As the input signals of difuzzifier is in voltage differential form so the transconductor circuit is used to apply the summation of input signals to current-input divider block.

A class-AB differential-input trasconductor circuit is shown in Fig .10 [4] in which the output current can be calculated as:

$$I_{out} = \beta(V_I + V_{eff})^2 \qquad (11)$$

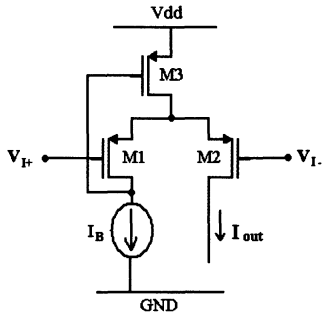

Fig. 10. Differential-input trasconductor circuit

Where $V_{I+}-V_{I-} \geq \sqrt{\frac{I_b}{\beta}}$ and $\beta = \frac{1}{2}\mu \cdot c_{ox}\frac{W}{L}$ is a MOSFET's transconductance parameter and $V_{ref} = \sqrt{\frac{I_B}{\beta}}$ is an effective voltage of M1 [4].

Fig.11 shows the class AB linear transconductor which is realized by cross-coupling pair of non-linear transconductors of Fig. 10. Assuming that M1-M4 are of identical dimensions, it can be found that for $V_I \leq \sqrt{\frac{I_B}{\beta}}$, the differential output current is linearly dependent on the differential input voltage that is shown in equation(12).[4]

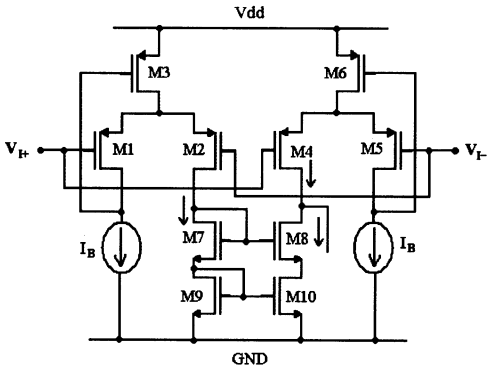

Fig. 11. Fully differential class-AB transconductor

$$I_{out} = I_{O1} - I_{O2} = 4V_I\sqrt{\beta \cdot I_B} \qquad (12)$$

Where $\beta = \beta_1 = \beta_2 = \beta_3 = \beta_4$. According to (12), it is clearly seen that the transconductance gain is a square-root function of the bias current I_B.

The total detailed bloke diagram of center of area difuzzifier method becomes as Fig .12.

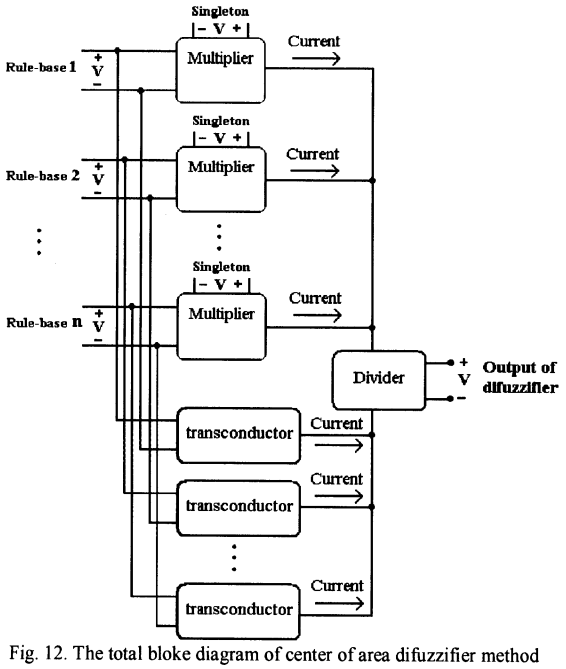

Fig. 12. The total bloke diagram of center of area difuzzifier method

Two input voltages X and Y applied to the multiplier and summation of output currents of multipliers is applied to divider and the other input of divider is the summation of trasconductors output current and the input of trasconductors are Xs as shown in Fig. 9, where X is output of rule-base and Y is singleton.

CONCLUSIONS

In this paper, a voltage-mode center of area defuzzifier circuit based on quarter-square multiplier and voltage-input current-output divider circuits is proposed. This circuit has been simulated with HSPICE. The experimental results indicate that the proposed circuit can work well. Besides the functional testing, its transient response is also tested. Rely on this design, a general purpose fuzzy processor can be achieved

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